REMARKS

Claims 1 and 5 are amended. Claim 2 and 6 are canceled. Claims 3-4 and 7-16 are withdrawn. Claims 1 and 3-16 are pending in the present application.

At the outset, Applicants respectfully request that the drawings be acknowledged as either accepted or objected to by the Examiner.

Claim 1 stands rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,121,666 ("Burr"). Applicants respectfully traverse this rejection.

Claim 1, as amended, recites a semiconductor apparatus including a MOS transistor, said MOS transistor comprising "a semiconductor substrate configured to provide a channel region between a source and a drain; . . . wherein a source side of the channel region has a first channel impurity density and a drain side of the channel region has a second channel impurity density different from the first channel impurity density, the difference in channel impurity density producing a threshold voltage of the source side region of the MOS transistor is higher than that of the drain side region in a longitudinal direction of the channel region." Burr does not disclose all the limitations of claim 1.

Burr discloses MOS devices having "a thin 'notch region' of their gate oxide adjacent to either the source or drain and lying over a region of the device's channel region that has been engineered to have a relatively 'high' threshold voltage . . . in comparison to the remainder of the channel region." Col. 3, lines 20-25. Burr further discloses that "[p]rovided within well region 34 are (1) a heavily doped n-type source region 36 with an associated 'tip' 36A, and (2) a corresponding heavily doped drain region 38 with an associated tip 38A." Col. 6, lines 52-55; Fig. 1a. Burr also discloses that a "channel region 44 is provided in the device 30 between the source and drain tip

regions 36A and 38A." Col. 7, lines 23-24; Fig. 1a. However, Burr is silent on a MOS transistor comprising "a semiconductor substrate configured to provide a channel region between a source and a drain; . . . *wherein a source side of the channel region has a first channel impurity density and a drain side of the channel region has a second channel impurity density different from the first channel impurity density,* the difference in channel impurity density producing a threshold voltage of the source side region of the MOS transistor is higher than that of the drain side region in a longitudinal direction of the channel region," as recited in claim 1. Emphasis added.

Since Burr does not disclose all the limitations of claim 1, claim 1 is patentable over Burr. Accordingly, Applicants respectfully request that the 35 U.S.C. § 102(b) rejection of claim 1 be withdrawn.

Claims 5 and 6 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Burr in view of U.S. Patent No. 3,877,055 ("Fisher"). Applicants respectfully traverse this rejection.

Claims 5 and 6 depend from claim 1. For at least the same reason as discussed above with respect to the patentability of claim 1 over Burr, Burr does not teach or suggest all the limitations of claim 1. Burr does not teach or suggest a MOS transistor comprising "a semiconductor substrate configured to provide a channel region between a source and a drain; . . . wherein a source side of the channel region has a first channel impurity density and a drain side of the channel region has a second channel impurity density different from the first channel impurity density, the difference in channel impurity density producing a threshold voltage of the source side region of the MOS transistor is higher than that of the drain side region in a longitudinal direction of the channel region," as recited in claim 1.

Fisher cannot supplement the inadequacy of Burr in this respect. Fisher discloses that "three diffused areas 32, 33 and 34, all having P-type conductivity, are formed in the substrate 30." Col. 3, lines 39-40; Fig. 3. Fisher further discloses that the "channel length of each of the MNOS devices is defined by the length of N-type conductivity substrate 30 between the diffused areas 32-33 and 33-34." Col. 4, lines 50-52; Fig. 9. However, Fisher is silent on a channel region wherein "a source side of the channel region has a first channel impurity density and a drain side of the channel region has a second channel impurity density different from the first channel impurity density," as recited in claim 1.

Since Burr and Fisher, whether considered alone or in combination, do not teach or suggest all the limitations of claim 1, claims 5 and 6 depending therefrom are patentable over the references. Accordingly, Applicants respectfully request that the 35 U.S.C. § 103(a) rejection of claims 5 and 6 be withdrawn.

Claims 1, 5 and 6 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Fisher in view of Burr. Applicants respectfully traverse this rejection.

For at least the same reasons as discussed above regarding the patentability of claims 1, 5 and 6 above over Burr in view of Fisher, claims 1, 2, 5 and 6 are likewise patentable over the disclosure of Fisher in view of Burr. Fisher and Burr, whether considered alone or in combination, do not teach or suggest all the limitations of independent claim 1. Fisher and Burr do not teach or suggest a MOS transistor comprising "a semiconductor substrate configured to provide a channel region between a source and a drain; . . . wherein a source side of the channel region has a first channel impurity density and a drain side of the channel region has a second channel impurity density different from the first channel impurity density, the difference in channel

impurity density producing a threshold voltage of the source side region of the MOS transistor is higher than that of the drain side region in a longitudinal direction of the channel region," as recited in claim 1. Since Fisher and Burr do not teach or suggest all the limitations of claim 1, claim 1 and claims 5 and 6 depending therefrom are patentable over the references. Accordingly, Applicants request that the 35 U.S.C. § 103(a) rejection of claims 1, 5 and 6 be withdrawn.

In view of the above amendment, Applicants believe the pending application is in condition for allowance.

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Respectfully submitted,

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